

Atsushi Kawasumi – U.S. Serial No. 10/760,474**REMARKS**

The Office Action of May 19, 2004, has been carefully reviewed and these remarks are responsive thereto. Reconsideration and allowance of the instant application are respectfully requested.

Claims 22 and 23 remain in this application.

Claim 23 has been amended.

Claim 24 has been added.

No new matter has been entered.

Objection to the Drawings

The drawings stand objected to. Filed under separate cover are new formal drawings that comport with the changes made in the parent application, US Serial No. 10/052,779. In particular, Figure 6 has been amended as suggested by the Examiner. A copy of new Figure 6 is attached hereto.

Rejection of Claims 22 and 23

Claims 22 and 23 stand rejected under 35 USC 112, second paragraph. Applicant traverses the rejection.

As to the rejection of claims 22 and 23 for the lacking connection between the subtractors and the gate and drain of the first PMOS transistors, Applicant submits this rejection is misplaced. There is no connection between the subtractors and the gate and drain of the first PMOS transistor.

The Examiner may be looking at Figures 4 and 6 where a diode connection exists on transistors. Applicant refers to Figures 16 and 18 respectively. As shown in Figures 16 and 18, there is no diode connection between a subtracted output of a subtractor and the first PMOS transistor 216₀. Rather, only voltage V_{g1} is applied to it. The subtractors are connected to the remainder of the PMOS transistors as shown by the subtracted input to 216_{1,2}. Accordingly, as there is no connection between the subtractors and the first PMOS transistor, Applicant submits that claim 22 is clear as written.

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As to claim 23, the same position applies. Here, the relevant figure includes figure 18. With respect to the agreement of the voltage circuit, Applicant has specifically indicated in claim 23 that the voltage circuit is the same voltage circuit.

Applicant has added new claim 24 that addresses claim 23 but with a second voltage circuit.

Applicant submits the application is in condition for allowance. If the Examiner has any questions, he is invited to contact the undersigned.

Respectfully Submitted,

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